APPENDIX U

1-150 (Cancelled).

151 (New). A memory device, comprising:

an array of dynamic random access memory cells;

a clock receiver to receive an external clock signal;

a register to store a value; and

a plurality of input receivers that includes input receivers to sample operation codes synchronously with respect to the external clock signal,

wherein a first operation code of the operation codes instructs the memory device to store the value in the register,

wherein a second operation code of the operation codes instructs the memory device to perform a write operation,

wherein, in response to the second operation code, the memory device samples write data corresponding to the write operation at a time determined using the value stored in the register, and

wherein the write data is stored in the array after being sampled.

152 (New). The memory device of claim 151, wherein the write data is sampled by the plurality of input receivers.

153 (New). The memory device of claim 152, wherein at least a portion of the write data is sampled by the input receivers of the plurality of input receivers that are also used to sample operation codes.

154 (New). The memory device of claim 152, wherein the memory device includes pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device, wherein, for a pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the external clock signal.

155 (New). The memory device of claim 152, wherein the memory device includes pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device, wherein, for each pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the external clock signal.

156 (New). The memory device of claim 151, wherein the write data is stored in the array at a location corresponding to address information, wherein the address information is sampled by the memory device synchronously with respect to the external

clock signal.

157 (New). The memory device of claim 156, wherein at least a portion of the address information is sampled by the plurality of input receivers.

158 (New). The memory device of claim 151, wherein the value stored in the register is also used in determining a time at which read data corresponding to a read operation is output by the memory device, wherein the read data is read from the array, and wherein a third operation code of the operation codes instructs the memory device to perform the read operation.

159 (New). The memory device of claim 158, wherein a difference between a time after which the memory device outputs the read data based on storage of a first value in the register and a time after which the memory device outputs the read data based on storage of a second value in the register is a whole number of clock cycles.

160 (New). The memory device of claim 159, wherein the time after which the memory device outputs the read data relative to the sampling of the third operation code is about the same as

the time after which the memory device samples the write data relative to the sampling of the second operation code.

161 (New). The memory device of claim 151, wherein a difference between the time after which the memory device samples the write data based on storage of a first value in the register and the time after which the memory device samples the write data based on storage of a second value in the register is a whole number of clock cycles.

162 (New). The memory device of claim 151, wherein the operation codes are included in request packets.

163 (New). A memory device, comprising:

an array of dynamic random access memory cells;

a clock receiver to receive an external clock signal;

a clock generation circuit coupled to the clock receiver, the clock generation circuit to generate an internal clock signal using the external clock signal, the clock generation circuit including:

a delay circuit to delay the external clock signal by a variable delay to produce a delayed clock signal; and

a comparison circuit, coupled to the delay circuit, to

adjust the variable delay based on a comparison between the delayed clock signal and the external clock signal;

a register to store a value;

a plurality of input receivers that includes input receivers to sample operation codes synchronously with respect to the external clock signal, wherein a first operation code instructs the memory device to store the value in the register, and wherein a second operation code instructs the memory device to perform a write operation, wherein, in response to the second operation code, the memory device samples an amount of write data corresponding to the write operation at a time determined using the value stored in the register, wherein the amount of write data sampled is determined using a block size value received by the memory device, wherein the write data is sampled synchronously with respect to the external clock signal, and wherein the write data is stored in the array after being sampled;

pads coupled to the plurality of input receivers, the pads to interface with signal lines external to the memory device, wherein, for each pad from which write data is sampled, the memory device samples two bits of write data from the pad during a clock cycle of the external clock signal; and

a plurality of output drivers coupled to the clock

generation circuit, wherein the memory device outputs read data using the plurality of output drivers during a read operation, wherein the read operation is specified by a third operation code, and wherein the memory device outputs read data using the internal clock signal.

164 (New). The memory device of claim 163, wherein the pads are located on one side of a die on which the memory device is formed.

165 (New). The memory device of claim 163, wherein each output driver of the plurality of output drivers is coupled to a respective pad of the pads.

166 (New). The memory device of claim 163, wherein the delay circuit includes a variable delay line and a fixed delay component.

167 (New). The memory device of claim 163, further including sense amplifiers, coupled to the array, to sense the read data, wherein the third operation code includes precharge information that indicates whether the sense amplifiers are to be precharged after the read data is sensed by the sense amplifiers.

168 (New). The memory device of claim 163, wherein the write data is stored in the array at a location corresponding to address information, wherein the address information is sampled by the memory device synchronously with respect to the external clock signal.

169 (New). The memory device of claim 168, wherein at least a portion of the address information is sampled by the plurality of input receivers.

170 (New). The memory device of claim 163, wherein the value is received by the plurality of input receivers.

171 (New). A method of operating a memory device, comprising:

receiving a first external clock signal;

generating an internal clock signal using the first external clock signal, wherein generating includes:

delaying the first external clock signal by a variable delay to produce a delayed clock signal;

comparing the delayed clock signal and the first external clock signal; and

adjusting the variable delay based on the comparison between the delayed clock signal and the first external clock signal;

receiving a value;

storing the value in a register on the memory device;

receiving a block size value that indicates an amount of data to be sampled during a write operation;

receiving a first operation code that indicates the write operation;

in response to the first operation code and after a write latency determined using the value stored in the register, sampling write data, wherein for a pad on the memory device from which write data is sampled, two bits of write data are sampled from the pad during a clock cycle of the first external clock signal;

storing the write data in an array of dynamic random access memory cells on the memory device;

receiving a second operation code that indicates a read operation, wherein the second operation code includes precharge information that indicates that the memory device should precharge sense amplifiers on the memory device;

in response to the second operation code and after a read latency determined using the value stored in the register,

outputting read data in response to the second operation code, wherein the read data is output using the internal clock signal; and

precharging sense amplifiers on the memory device in response to the precharge information included in the second operation code.

172 (New). The method of claim 171, wherein sampling write data further comprises sampling, from each pad on the memory device from which write data is sampled, two bits of write data during a clock cycle of the first external clock signal.

173 (New). The method of claim 171, further comprising receiving a third operation code, and wherein storing the value in the register further comprises storing the value in the register in response to the third operation code.

174 (New). The method of claim 173, further comprising receiving address information, wherein storing the write data further comprises storing the write data in a location of the array based on the address information.

175 (New). The method of claim 173, wherein generating the

internal clock signal further comprises:

receiving a second external clock signal; and

generating the internal clock signal using the first and second external clock signals.

176 (New). The method of claim 175, wherein generating the internal clock signal further comprises generating the internal clock signal such that transitions of the internal clock signal occur about midway between corresponding transitions of the first and second external clock signals.

177 (New). A method of operating a memory device, comprising:

receiving an external clock signal;

generating an internal clock signal using the external clock signal, wherein generating includes:

delaying the external clock signal by a variable delay to produce a delayed clock signal;

comparing the delayed clock signal and the external clock signal; and

adjusting the variable delay based on the comparison between the delayed clock signal and the external clock signal;

receiving a value;

storing the value in a register on the memory device;

receiving a block size value that indicates an amount of data to be sampled during a write operation;

receiving a first operation code that indicates the write operation;

in response to the first operation code and after a write latency determined using the value stored in the register, sampling write data, wherein for each pad on the memory device from which write data is sampled, two bits of write data are sampled from the pad during a clock cycle of the external clock signal;

storing the write data in an array of dynamic random access memory cells on the memory device;

receiving a second operation code that indicates a read operation, wherein the second operation code includes precharge information;

in response to the second operation code and after a read latency determined using the value stored in the register, outputting read data in response to the second operation code, wherein the read data is output using the internal clock signal;

if the precharge information included in the second operation code indicates that a precharge function should be performed, precharging sense amplifiers on the memory device in

response to the precharge information included in the second operation code; and

if the precharge information included in the second operation code indicates that a precharge function should not be performed, holding data sensed in the sense amplifiers on the memory device.